

# MATLAB EXPO 2019

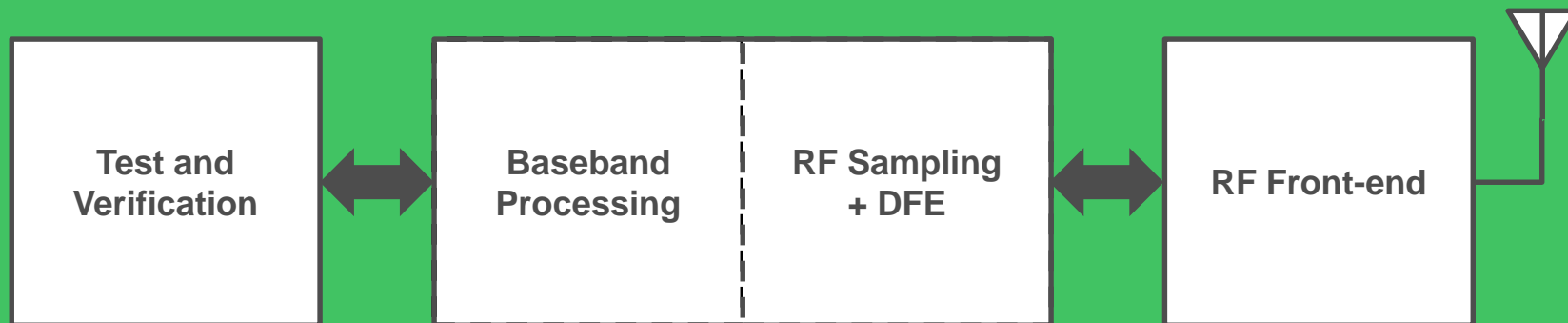
Verify 5G System Performance  
Using Xilinx RFSoc and  
Avnet RFSoc Development Kit

Matt Brown



# Elements of an RF Development System

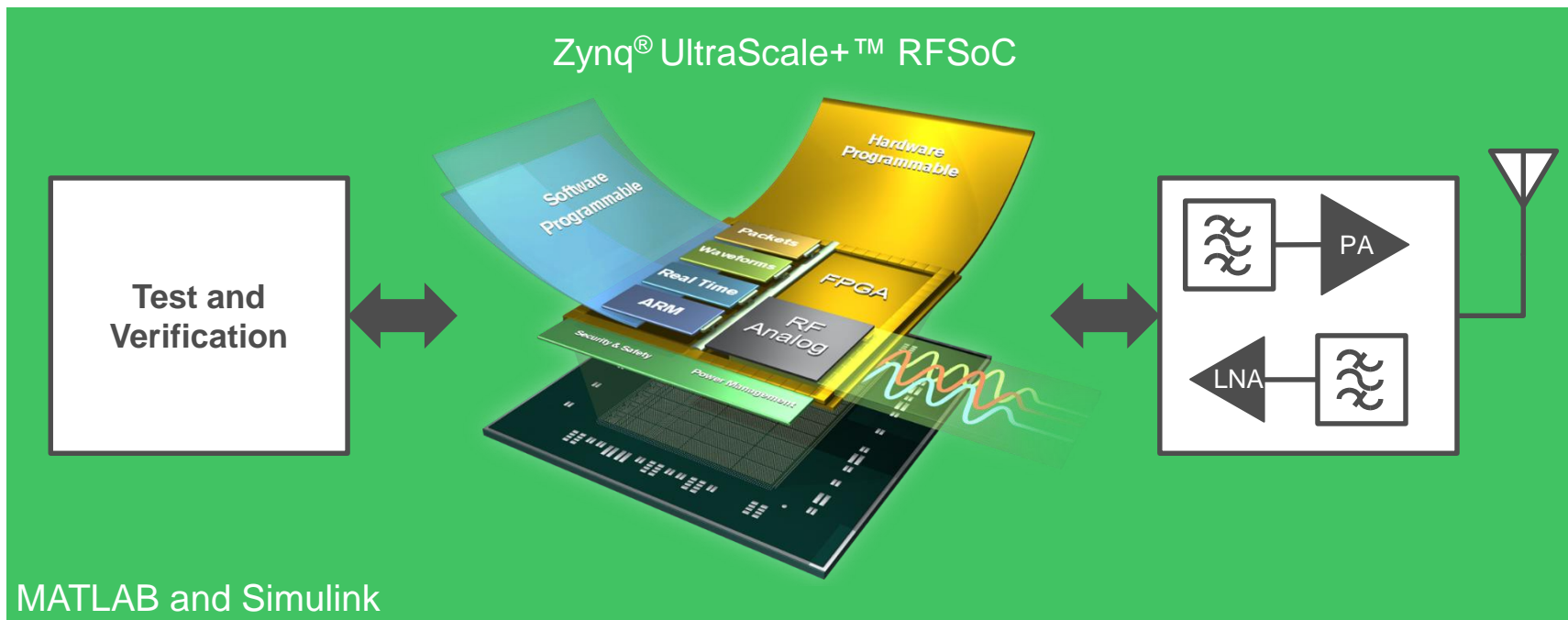
Modeling and simulation of the entire signal chain



MATLAB and Simulink

# Elements of an RFSoc Development System

Modeling and simulation of the entire signal chain



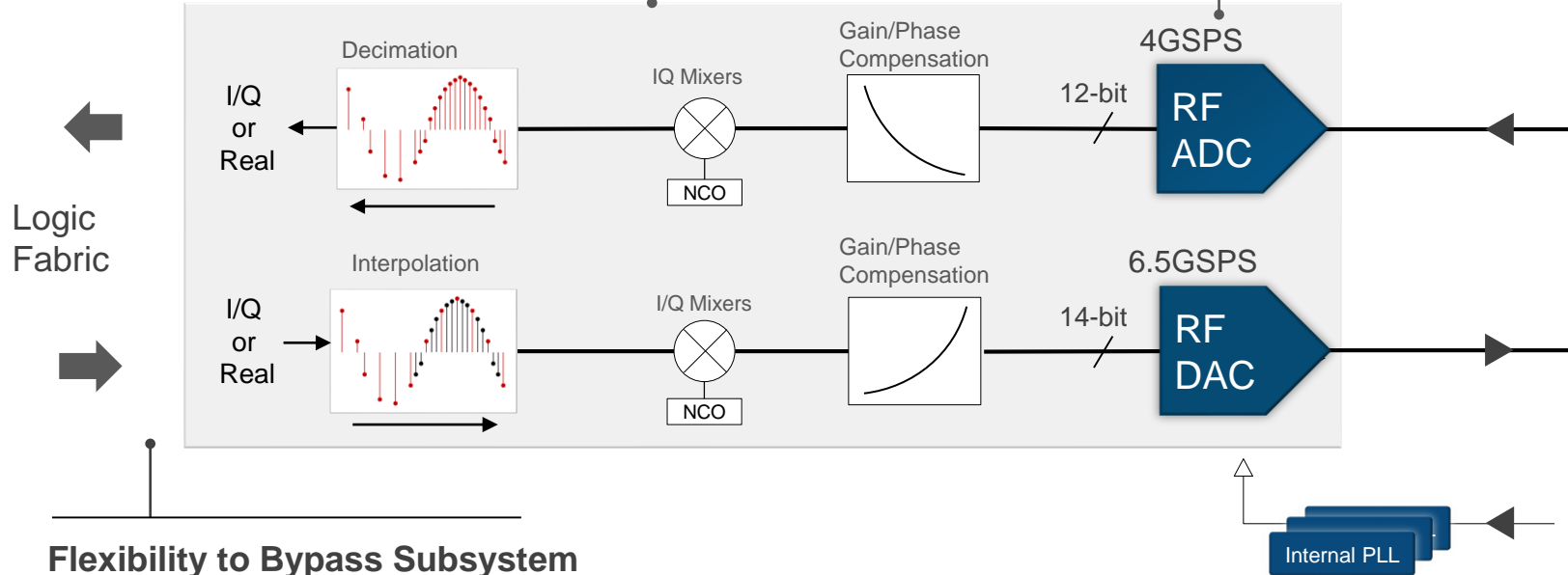
# Signal Processing from RF Front-End to Digital

## Digital Mixing and Filtering

- A complete DSP subsystem
- Digital Up-Conversion and Down-Conversion

## Direct-Sampling

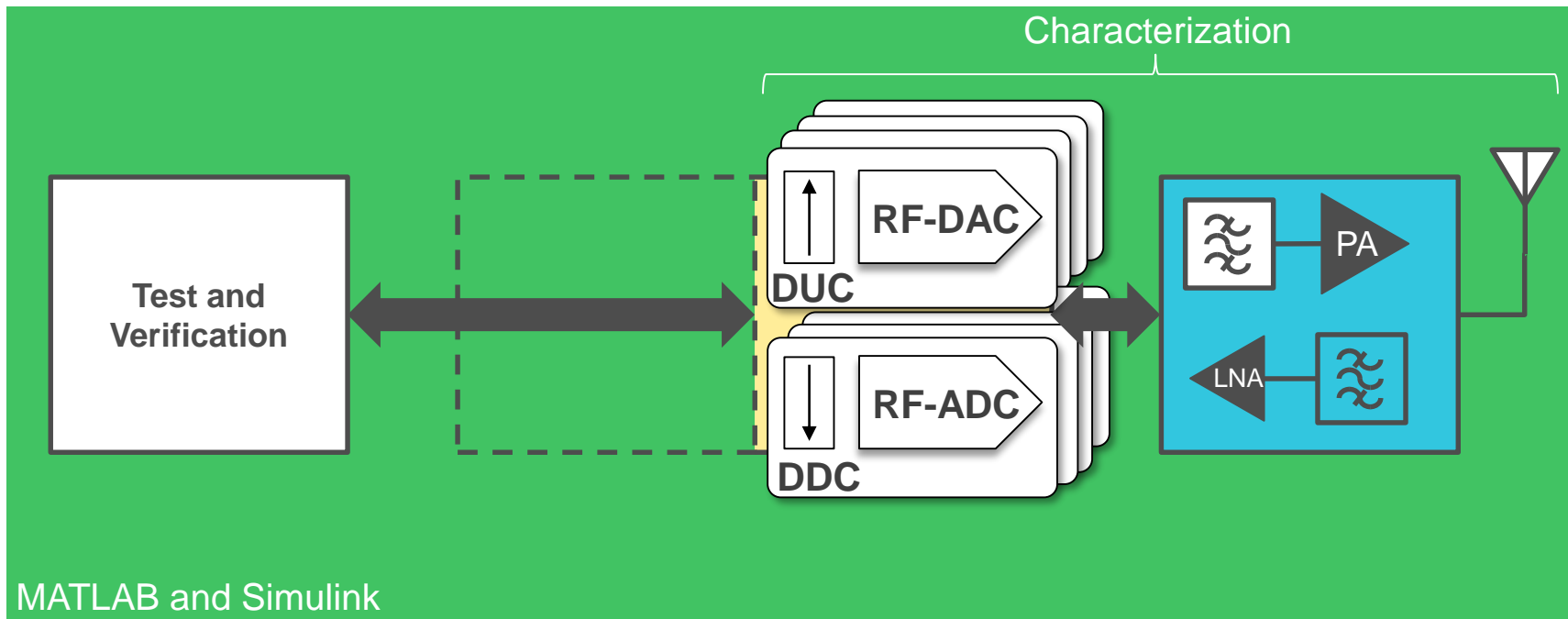
- High channel count
- Multiple Configurations



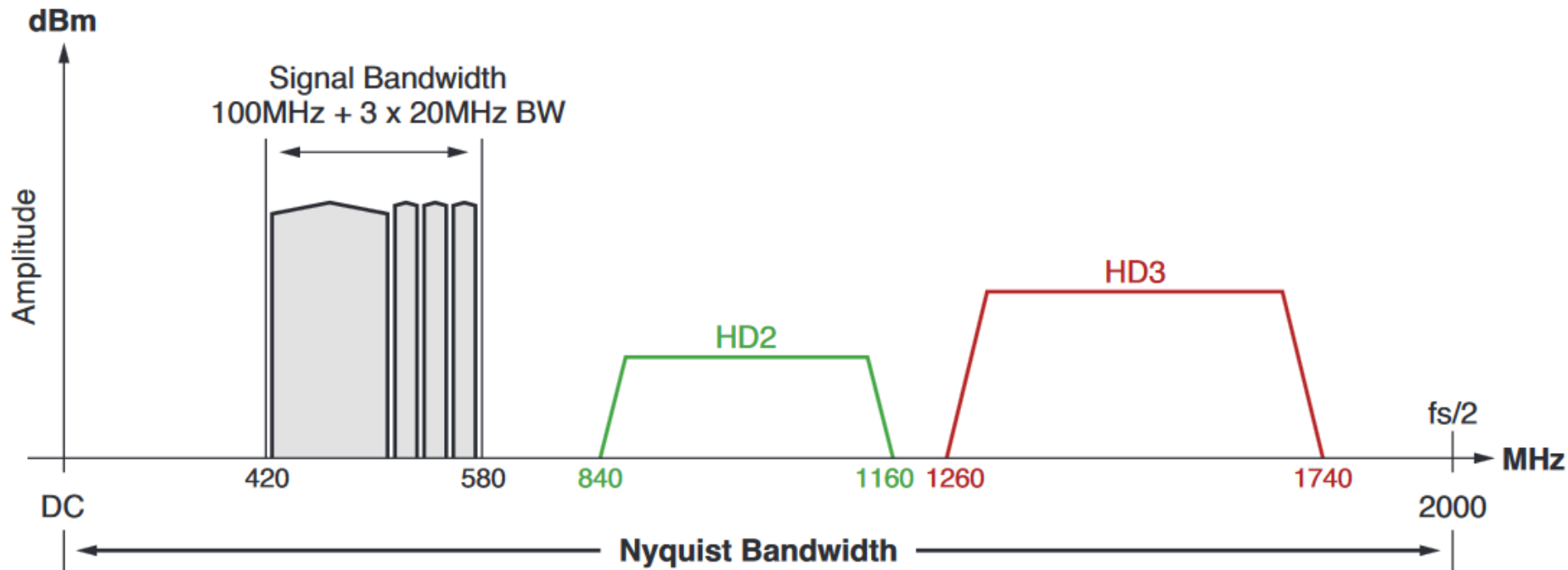
## Communication-Grade PLLs

Utilize lower frequency on-board clocks

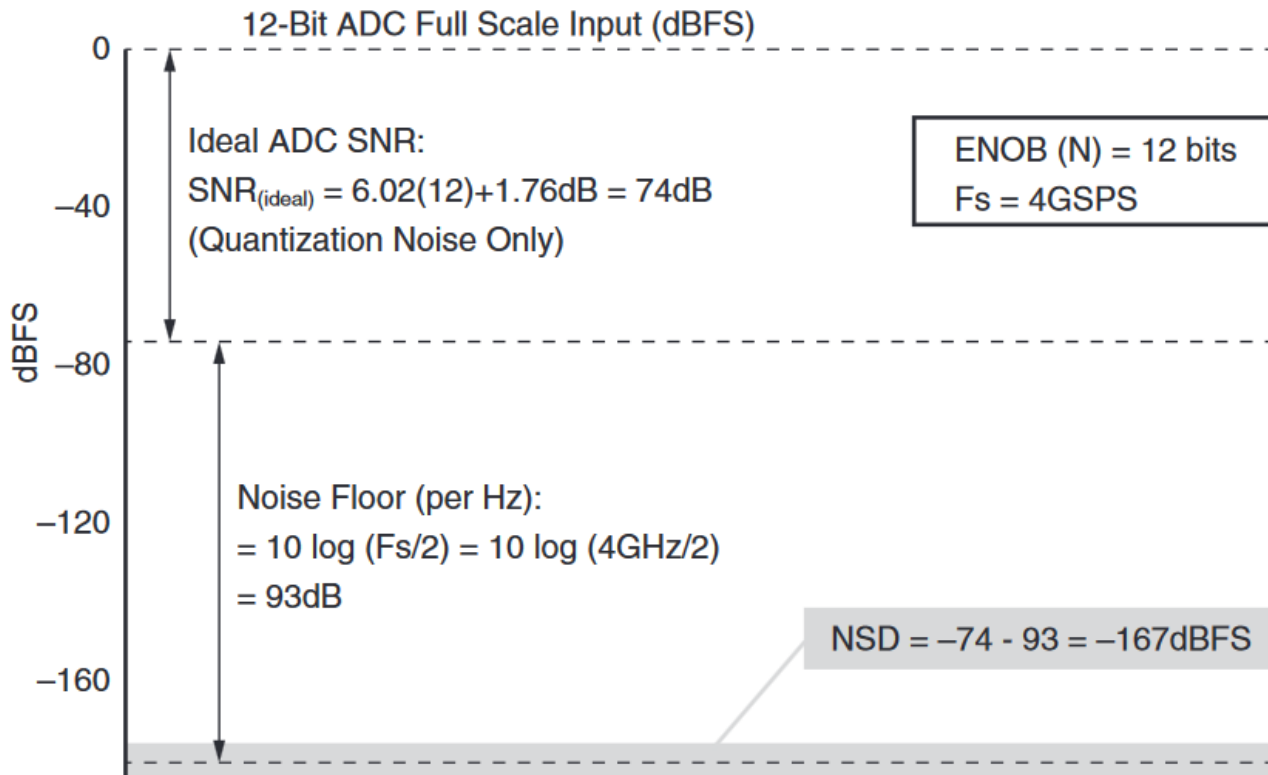
# How Do We Characterize RF Hardware?



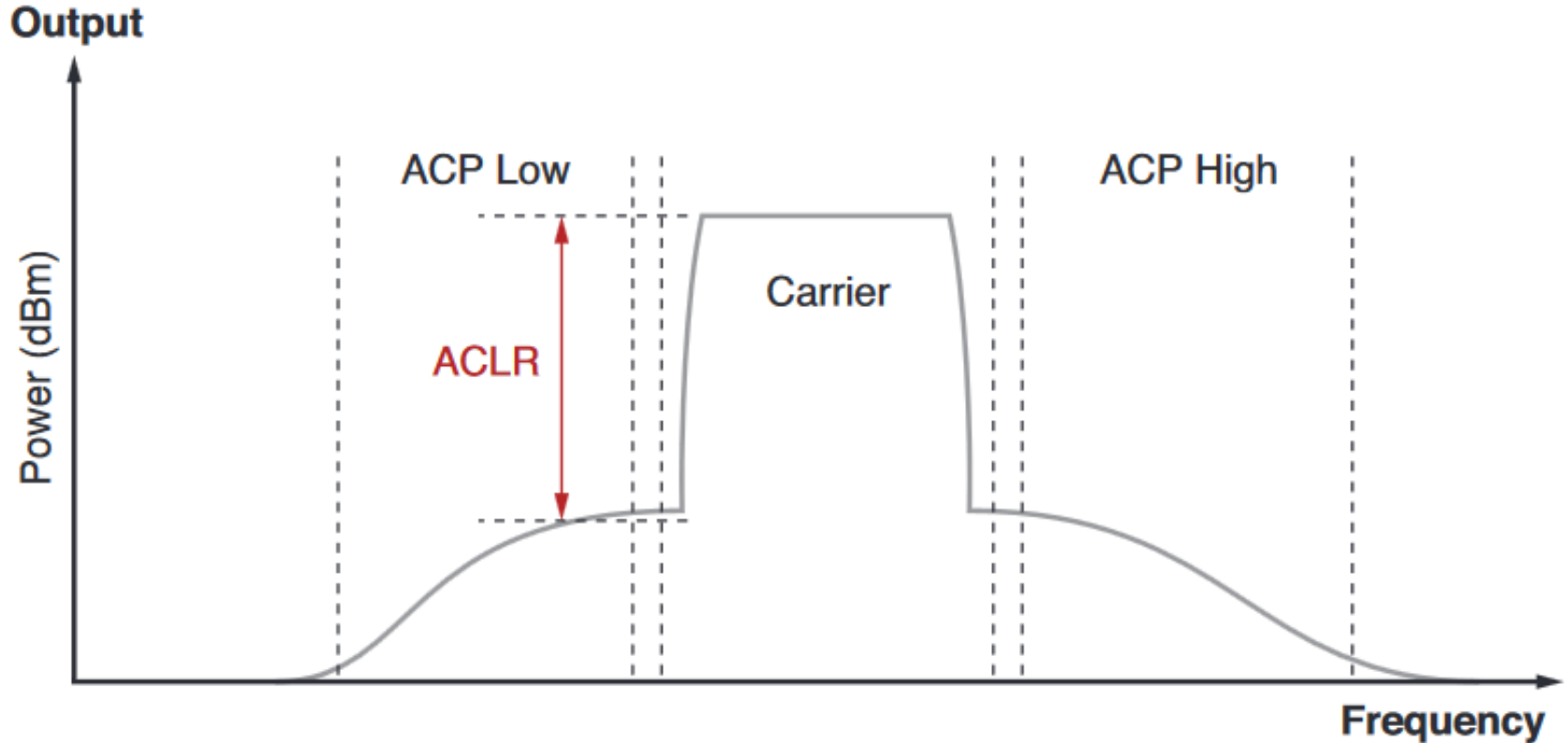
# Characterize 5G NR at the Band of Interest



# Noise Spectral Density

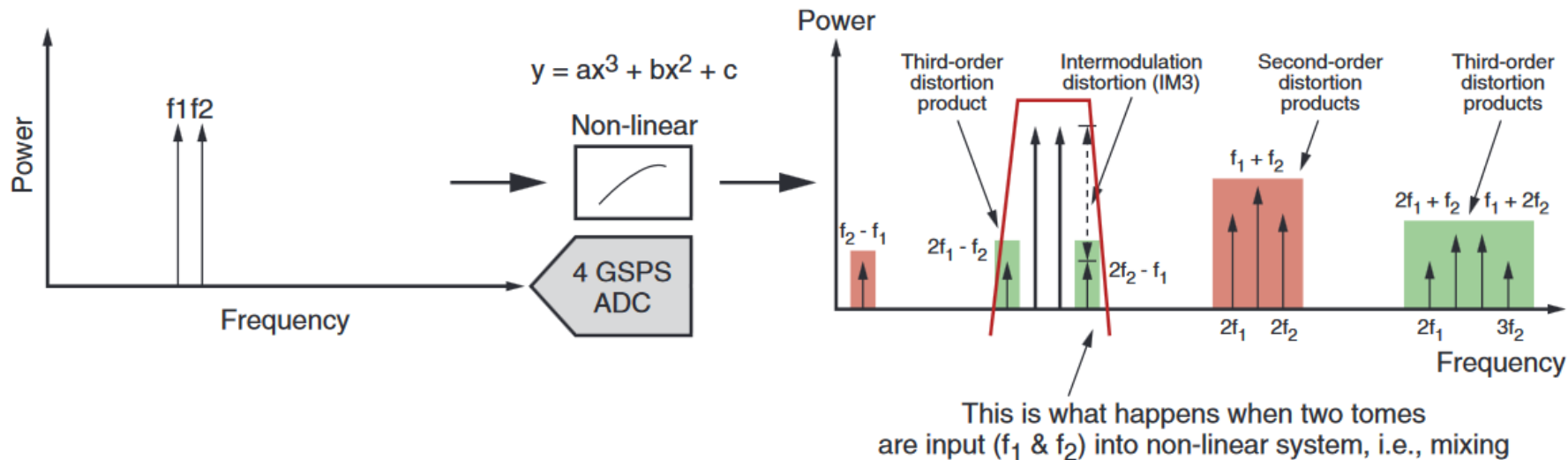


# Adjacent Channel Leakage Ratio (ACLR)



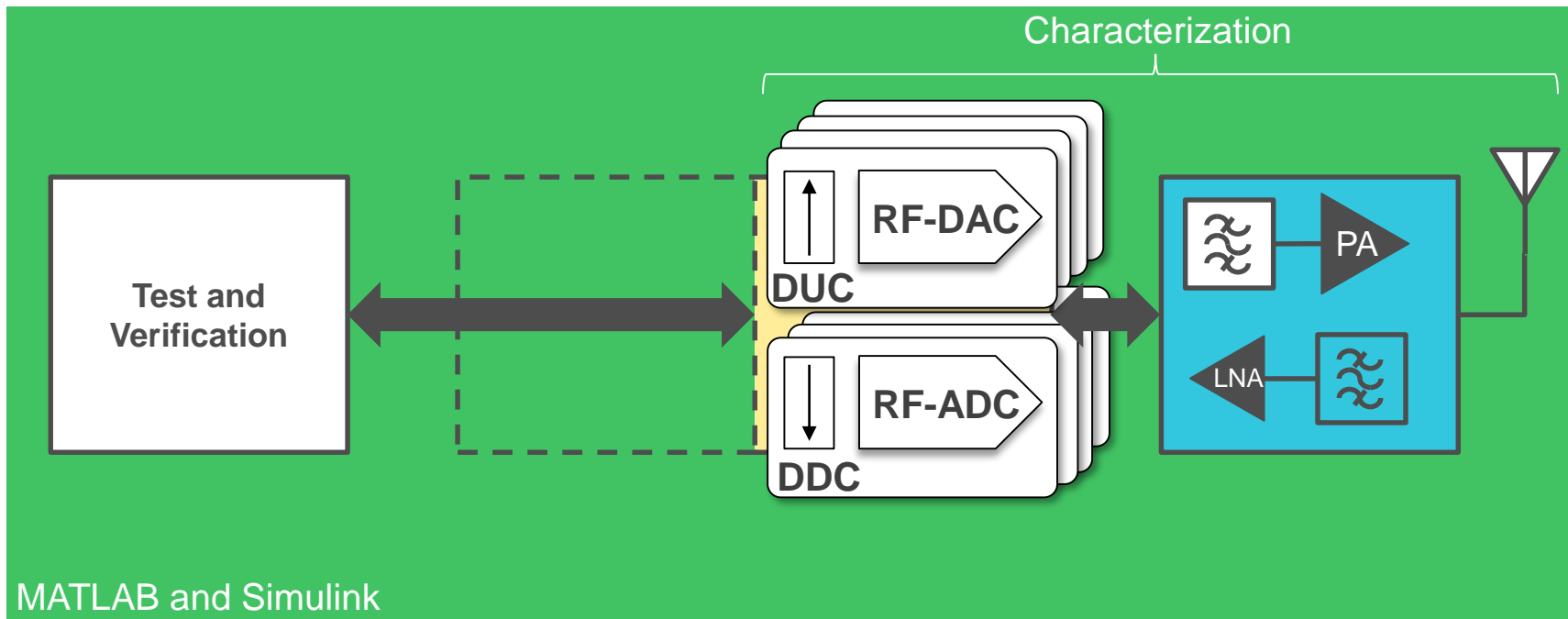


# IM3



WP509\_08\_010719


# How Do We Characterize RF Hardware?



# Avnet Products & Emerging Technologies Group



Prototyping  
with SoCs can  
be easier



Abstract the  
hardware using  
a suitable  
language



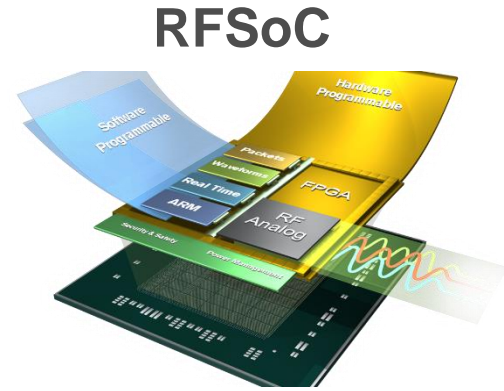
Deliver an  
intuitive app  
built natively in  
MATLAB®

# A History of SoC Abstraction

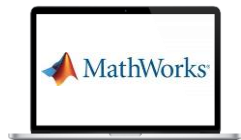
2010

2016

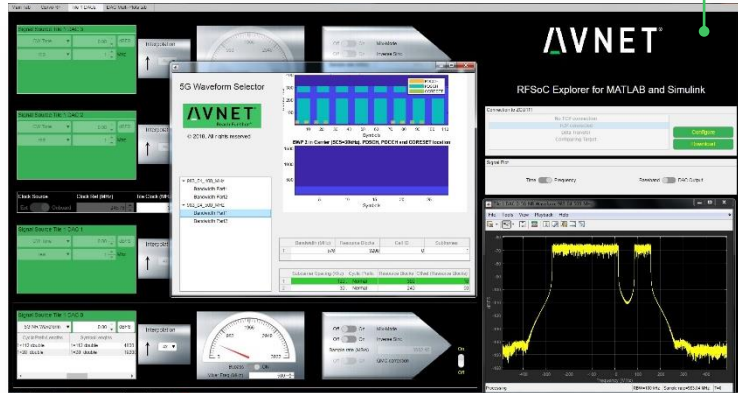
2019



# Explore Zynq UltraScale+ RFSoc from Antenna to Digital

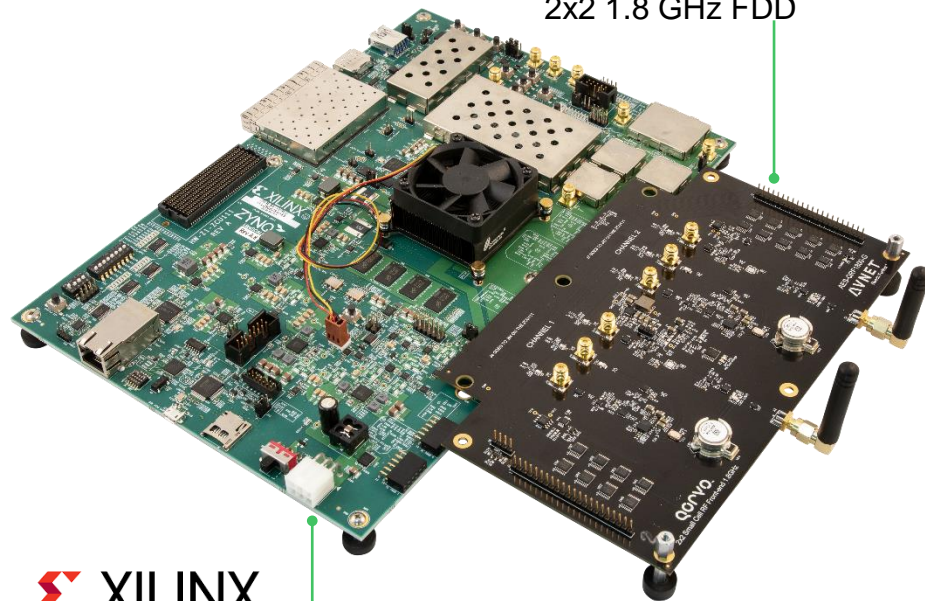


**AVNET**  
RFSoc Explorer®



**QORVO**

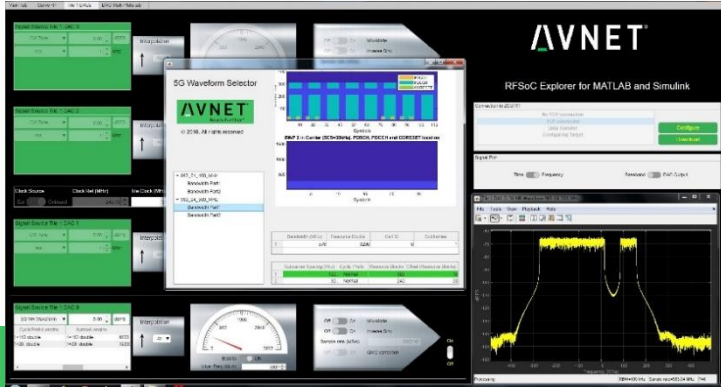
Small Cell RF Front End  
2x2 1.8 GHz FDD



**XILINX**

Zynq® UltraScale+™ RFSoc  
ZCU111 Evaluation Kit

# Abstracting the Hardware

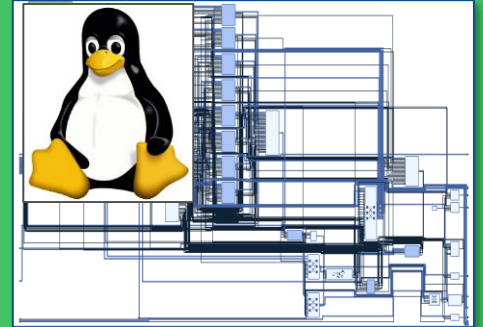


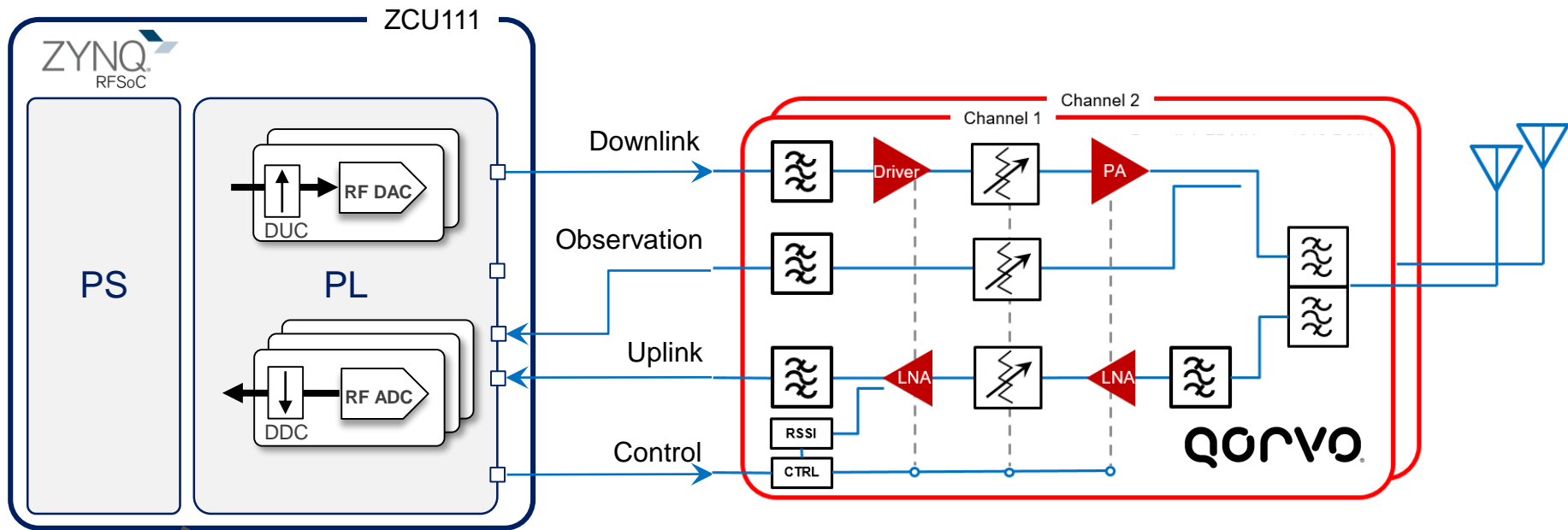
MATLAB  
System  
Objects

```
classdef AddOne < matlab.System
    % ADDONE Compute an output value that

    methods (Access = protected)
        % Implement algorithm. Calculate
        function y = stepImpl(~,x)
            y = x + 1;
        end
    end
end
```

Custom  
Boot  
Image





Gigabit Ethernet





# RFSoc Explorer for MATLAB and Simulink

**Signal Source Tile 1 DAC 3**

CW Tone  dBFS

complex  MHz

Interpolation

↑



Mix-Mode  On

Inverse Sinc  On

Sample rate (MS/s)

QMC correction  On

On

Off

**Signal Source Tile 1 DAC 2**

CW Tone  dBFS

complex  MHz

Interpolation

↑



Mix-Mode  On

Inverse Sinc  On

Sample rate (MS/s)

QMC correction  On

On

Off

Connection to ZCU111

- No TCP connection
- TCP connected
- Data Transfer
- Configuring Target

Signal Plot

Time  Frequency  Spectrum Analyzer

Baseband  DAC Output

**Clock Source**  Ext  Onboard

**Clock Ref (MHz)**

**Tile Clock (MHz)**

**Internal PLL**  Bypass  Enable

**Signal Source Tile 1 DAC 1**

CW Tone  dBFS

complex  MHz

Interpolation

↑



Mix-Mode  On

Inverse Sinc  On

Sample rate (MS/s)

QMC correction  On

On

Off

**Signal Source Tile 1 DAC 0**

CW Tone  dBFS

complex  MHz

Interpolation

↑



Mix-Mode  On

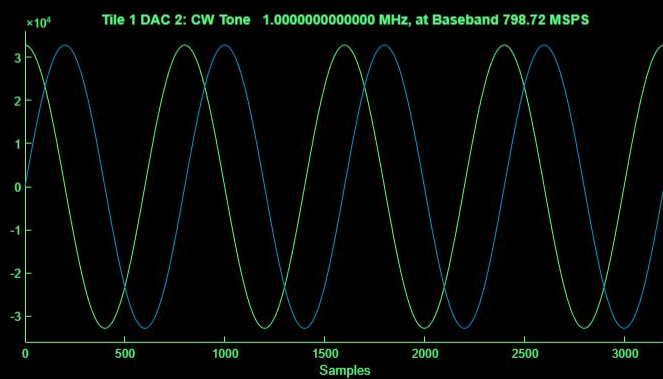
Inverse Sinc  On

Sample rate (MS/s)

QMC correction  On

On

Off





AVNET®

## RFSoc Explorer for MATLAB and Simulink

Connection to ZCU111

No TCP connection

TCP connected

Data Transfer

Configuring Target

Configure

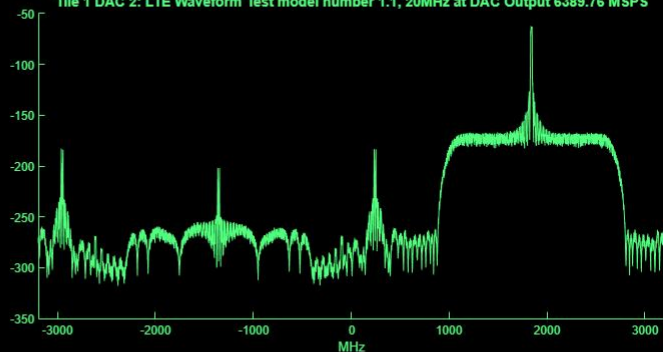
Download

Signal Plot

Time  FrequencyOff  OnBaseband  DAC Output

Spectrum Analyzer

Tile 1 DAC 2: LTE Waveform Test model number 1.1, 20MHz at DAC Output 6389.76 MSPS



LTE Downlink E-TM Generator

Generate downlink test model (E-TM) waveforms. These are specified in TS36.141 (section 6) for testing the downlink transmitter characteristics.

Test model

Bandwidth

Cell identity

Duplex mode

Number of subframes

Windowing (samples)

Waveform output variable

Resource grid output variable

E-TM configuration output variable

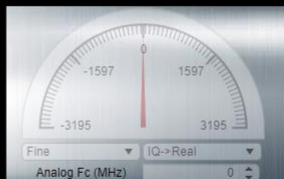
Signal Source Tile 1 DAC 3

CW Tone  dBFS

complex  Mhz

Interpolation

↑



Off  On Mix-Mode

Off  On Inverse Sinc

Sample rate (MS/s)

Off  On QMC correction

On

Off

Signal Source Tile 1 DAC 2

LTE Waveform  dBFS

TMN	BW	NDLRB	Cell
1.1	20MHz	100	1

Interpolation

↑



Off  On Mix-Mode

Off  On Inverse Sinc

Sample rate (MS/s)

Off  On QMC correction

On

Off

Clock Source

Ext  Onboard

Clock Ref (MHz)

Tile Clock (MHz)

Internal PLL

Bypass  Enable

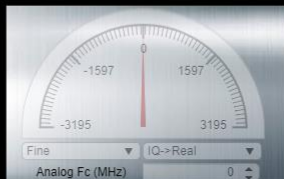
Signal Source Tile 1 DAC 1

CW Tone  dBFS

complex  Mhz

Interpolation

↑



Off  On Mix-Mode

Off  On Inverse Sinc

Sample rate (MS/s)

Off  On QMC correction

On

Off

Signal Source Tile 1 DAC 0

CW Tone  dBFS

complex  Mhz

Interpolation

↑



Off  On Mix-Mode

Off  On Inverse Sinc

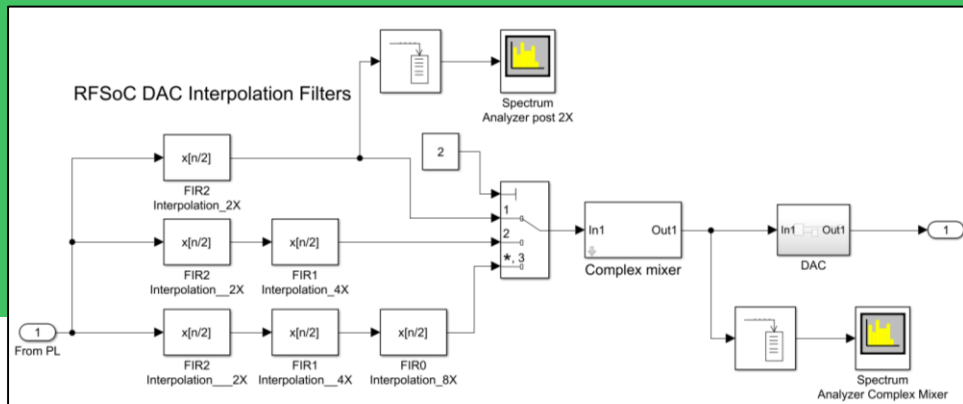
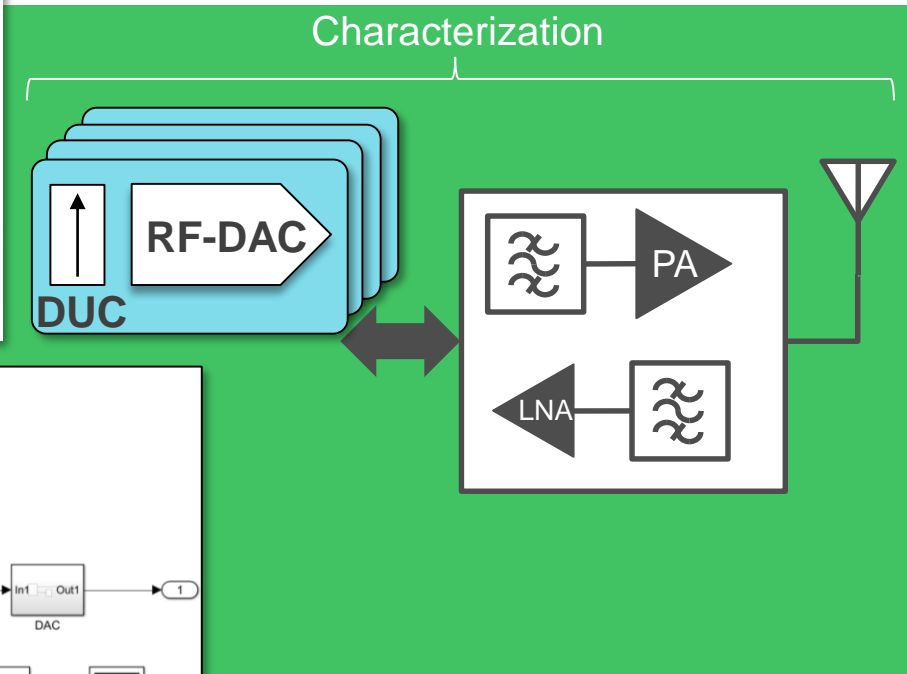
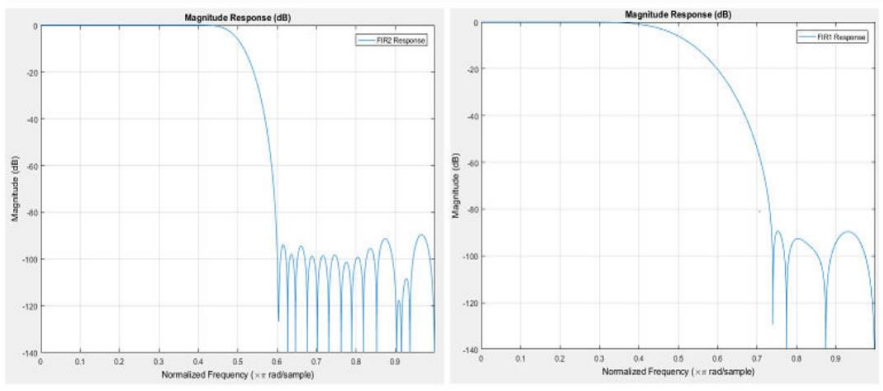
Sample rate (MS/s)

Off  On QMC correction

On

Off

# Modeling the Digital Up-Converter in RF-DAC Tile





## RFSoc Explorer® for MATLAB and Simulink

**ADC23**

ADC ENable  Off  On

Sample rate (MS/s) 1081.3440

Nyquist Zone 4

Calibration Mode 2

Analog Fc (MHz) 1842

NCO Freq MHz -1842

NCO Phase deg 0

Fine Real->IQ

Decimation

8x

Connection to ZCU111

- No TCP connection
- TCP connected
- Data Acquisition
- Configuring Target

Configure

Acquire

Single capture

Clock Source  Ext  Onboard

Clock Ref (MHz) 245.76

Tile Clock (MHz) 1081.344

**ADC01**

ADC ENable  Off  On

Sample rate (MS/s) 1081.3440

Nyquist Zone 1

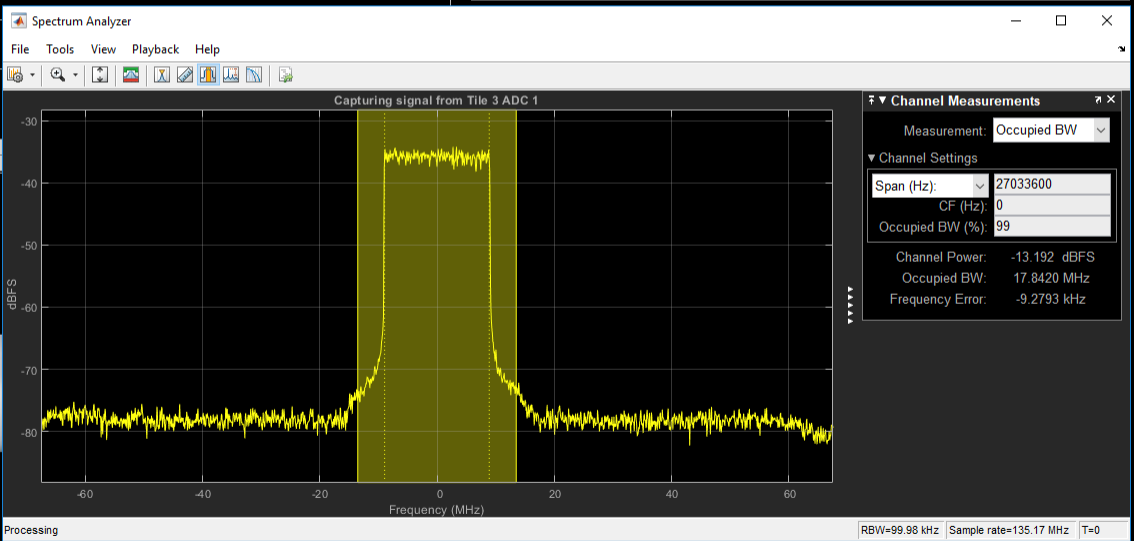
Calibration Mode 2

Analog Fc (MHz) -0

NCO Freq MHz 0

NCO Phase deg 0

Fine Real->IQ





# RFSoc Explorer for MATLAB and Simulink

**Signal Source Tile 1 DAC 3**

CW Tone  -Inf  dBFS

complex  1  MHz

Interpolation

↑ 4x



Off  On Mix-Mode

Off  On Inverse Sinc

Sample rate (MS/s) 6389.76

Off  On QMC correction

On

Off

**Signal Source Tile 1 DAC 2**

5G NR Waveform  0.00  dBFS

CW Tone Native Sampling Rate Nfft

LTE Waveform 983.0400 8192

Wireless Waveform 983.0400 32768

5G NR Waveform

MATLAB File

From PL DUT

From Simulink Model

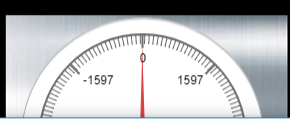
Clock Ref (MHz) 245.76

Tile Clock (MHz) 6389

Ext  Onboard

Interpolation

↑ 8x



Off  On Mix-Mode

Off  On Inverse Sinc

Sample rate (MS/s) 6389.76

On

Connection to ZCU111

No TCP connection

TCP connected

Data Transfer

Configuring Target

Signal Plot

Time  Frequency

Off  On Spectrum Analyzer

Baseband  DAC Output

**5G Waveform Selector**

AVNET Reach Further™

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▼ 983\_04\_400\_MHz

- Bandwidth Part1
- Bandwidth Part2

▼ 983\_04\_500\_MHz

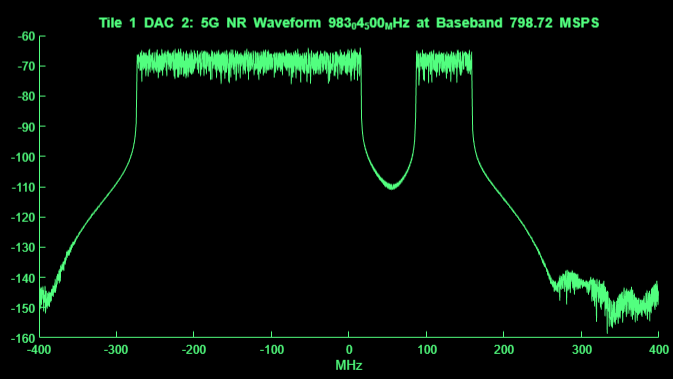
- Bandwidth Part1
- Bandwidth Part2

**BWP 1 in Carrier (SCS=120kHz), PDSCH, PDCCH and CORESET location**

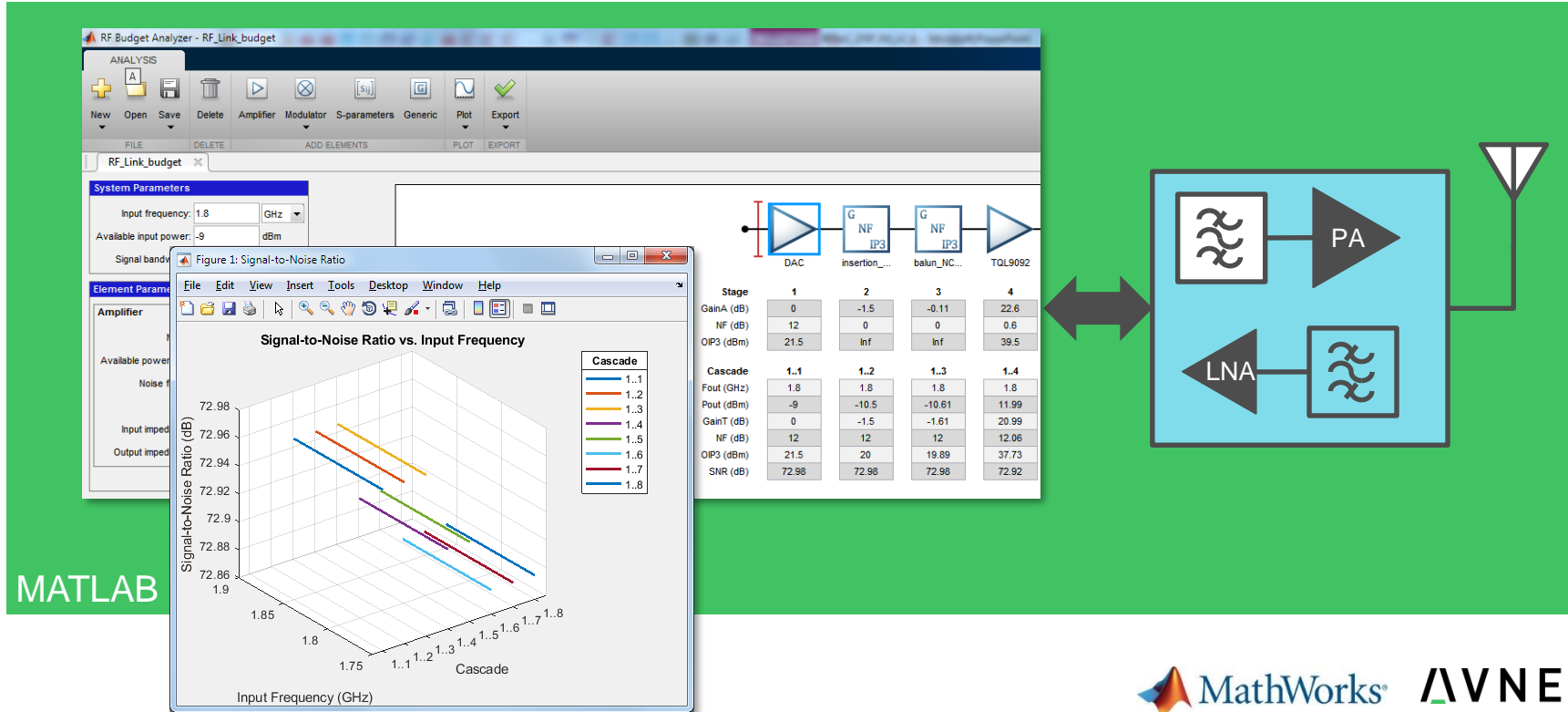
**BWP 2 in Carrier (SCS=30kHz), PDSCH, PDCCH and CORESET location**

Bandwidth (MHz)	Resource Blocks	Cell ID	Subframes
1	504	2800	0

Subcarrier Spacing (KHz)	Cyclic Prefix	Resource Blocks	Offset (Resource Blocks)
1	120	Normal	300
2	30	Normal	100

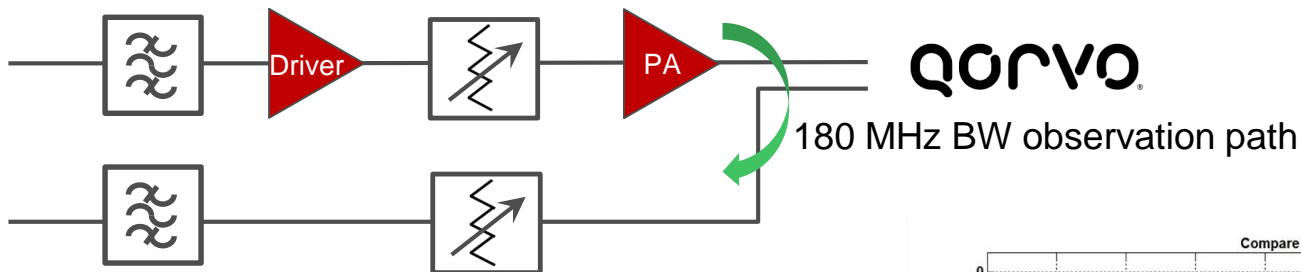


# RF Link Budget Analysis of Qorvo Front End

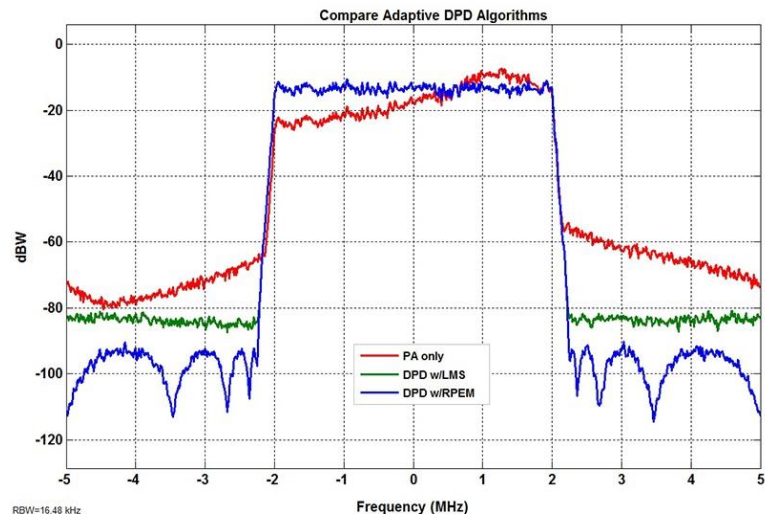
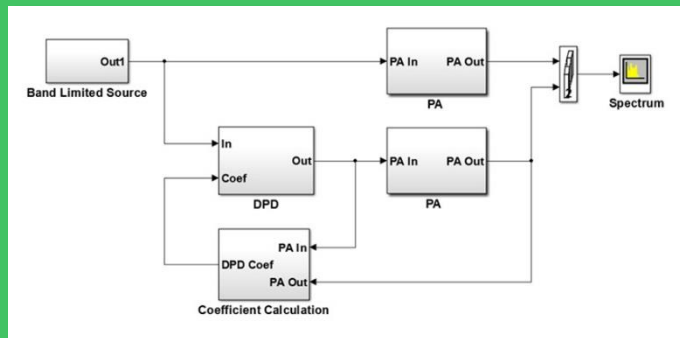


MATLAB

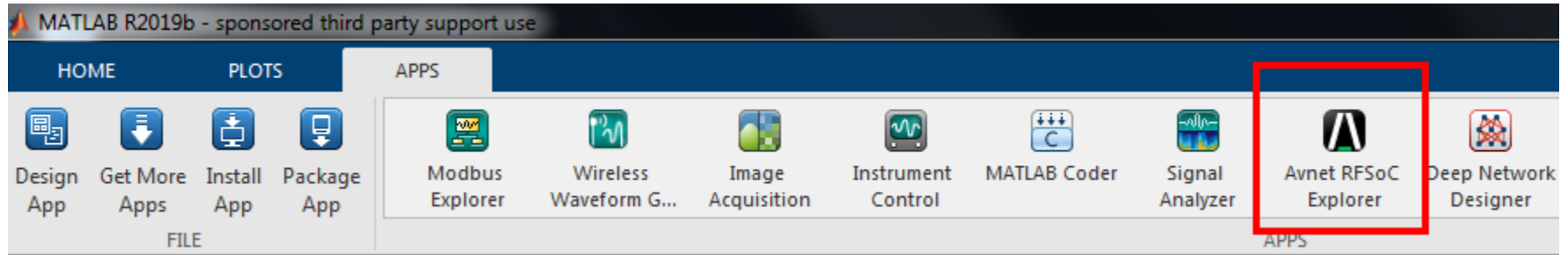
# Next ... Digital Pre-Distortion to Linearize the PA



## Simulink Adaptive DPD Modeling



# RFSoc Explorer in MATLAB Apps Store



[avnet.com / rfsocket](http://avnet.com/rfsocket)

Installation – MATLAB Apps & Add-Ons

Requires – Communications Toolbox Support Package for Xilinx Zynq-Based Radio

Free MATLAB Trial Package for Wireless Communications @ [mathworks.com/rfsoc](http://mathworks.com/rfsoc)

# MATLAB EXPO 2019

Thank You!

